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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/008,531	01/16/98	RHODES H	MI0012V2

MMC1/1024
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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 10/24/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

Office Action Summary	Application No. 09/008,531	Applicant(s) RHODES, HOWARD E.	
	Examin r Kurt M. Eaton	Art Unit 2823	

-- Th MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *07 August 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 21-24, 31-34, 40-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsuo et al..

In re claim 21, Matsuo et al. (herein referred to as Matsuo) shows in Figures 2A-2E and related text, a process for making a semiconductor device including the steps of forming a layer of conductive material (22) having a topography that includes a substantially vertical component; and forming a contact (13) disposed adjacent to and contacting the vertical component {see Figure 2B}.

In re claim 23, Matsuo shows wherein the vertical component is a spacer {see Figure 2B}.

In re claim 24, Matsuo further includes the step of forming a structure (21) having an opening therein under the conductive layer and filling the opening with the conductive material to form the vertical component {see Figure 2B}.

In re claim 31, Matsuo shows in Figures 2A-2E and related text, a process for making a semiconductor device including the steps of forming a conductive layer (22) having a topography that includes a substantially vertical component; forming a contact (13) disposed adjacent to and contacting the vertical component; and forming a structure (21) having an opening therein under the conductive layer and filling the opening with the conductive material to form the vertical component {see Figure 2B}.

In re claims 22 and 32, Matsuo shows wherein the vertical component defines a localized thick region in the layer of conductive material {see Figure 2B}.

In re claim 33, Matsuo shows in Figures 2A-2E and related text, a process for making a semiconductor device including forming a layer of conductive material (22) having a topography that includes a spacer; and forming a contact (13) disposed adjacent to and contacting the spacer{see Figure 2B}.

In re claim 34, Matsuo further includes the step of forming a structure (21) having an opening therein under the conductive layer and filling the opening with the conductive material to form the spacer {see Figure 2B}.

In re claim 40, Matsuo shows in Figures 2A-2E and related text, a process for making a semiconductor device including forming a conductive layer (22) having a thick region; and forming a contact (13) physically in contact with the thick region {see Figure 2B}.

In re claim 41, Matsuo shows wherein forming a conductive layer having a thick region includes forming a layer of conductive material having a thick region having a width greater than other portions of the conductive layer {see Figure 2B}.

In re claim 42, Matsuo shows wherein forming a conductive layer having a thick region includes forming a layer of conductive material having a thick region having a width greater than

other portions of the conductive layer and a depth extending below the other portions of the conductive layer {see Figure 2B}.

4. Claims 26-28, 30, 35, 36, 44 and 45 are rejected under 35 U.S.C. 102(e) as being anticipated by Bergemont.

In re claim 26, Bergemont shows in Figures 10 and 12-14 a process for making a semiconductor device having an improved contact to a conductive layer including the steps of providing a first layer of material (118) and forming an opening therein, wherein the opening includes sidewalls (119); forming a layer of a first conductive material (122) on the first layer of material and along the surfaces of the sidewalls of the opening to form a localized thick region; forming an overlayer of material (124) on the layer of the first conductive material; forming a contact hole in the overlayer of material on the layer of the first conductive material; and substantially filling the contact hole in the overlayer with a second conductive material (126) which differs in composition from the first conductive layer and which contacts the first conductive material {column 8, line 56 – column 10, line 9}.

In re claim 27, Bergemont shows where the first conductive material forms spacers on the sidewalls of the opening {see Figure 13}.

In re claim 28, Bergemont shows where the second conductive material contacts at least the spacers {see Figure 14}.

In re claim 35, Bergemont shows in Figures 10 and 12-14 a process for making a semiconductor device having an improved contact to a conductive layer including providing a first layer of material (118) and forming an opening therein, wherein the opening includes sidewalls (119); forming a layer of first conductive material (122) on the first layer of material and wherein the first conductive material forms spacers on the sidewalls; forming an overlayer of material (124) on the

layer of the first conductive material; forming a contact hole in the overlayer which communicates with the layer of the first conductive material; and substantially filling the contact hole in the overlayer with a second conductive material (126) which differs in composition from the first conductive layer and which contacts at least the spacers {column 8, line 56 – column 10, line 9}.

In re claims 30 and 36, Bergemont shows where the first layer and the overlayer include insulating materials {column 8, line 56 – column 10, line 9}.

In re claim 44, Bergemont shows in Figures 10 and 12-14 a process for making a semiconductor device including forming a layer of conductive material (122) having at least one thick component; and forming at least one contact (126) wherein each of the at least one contact is in contact with one of the at least one thick component {column 8, line 56 – column 10, line 9}.

In re claim 45, Bergemont shows in Figures 10 and 12-14 a process for making a semiconductor device including forming an underlayer (118) over a substrate; etching at least a portion of the underlayer to form an opening; and forming a conductive layer (122) over the underlayer and forming a thick region of the conductive layer over the opening {column 8, line 56 – column 10, line 9}.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo, as applied to claim 21 above.

Matsuo shows wherein the contact disposed adjacent to and contacting the vertical component is a capacitor electrode made of the same material as the layer of conductive material {column 4, lines 3-22}.

Matsuo fails to show wherein the layer of conductive material is a capacitor electrode.

It would have been obvious to one of ordinary skill in the art at the time the invention was made that the layer of conductive material and the contact, which is a capacitor electrode, of Matsuo were in electrical contact with each other. Accordingly, it would have been obvious that the layer of conductive material of Matsuo could have been considered a part of the capacitor electrode since, as far as the function of a capacitor is concerned, there exists no electrical boundary between the layer of conductive material and the contact, which is a capacitor electrode.

7. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo, as applied to claim 40 above, in view of Wolf et al..

Matsuo shows in Figure 2B wherein forming the contact includes forming an oxide layer (23) over the conductive layer, wherein the conductive layer is made of polysilicon; and forming an opening in the oxide layer; and forming the contact physically in contact with the thick region {column 3, line 59 – column 5, line 55}.

Matsuo does not show wherein forming the contact includes etching a tolerable amount of the thick region and forming the contact physically in contact with the thick region at a depth deeper than an upper surface of the thick region.

Wolf et al. (herein referred to as Wolf) teaches, in an analogous art related to dry etching for VLSI fabrication, that oxide may be etched selectively to polysilicon material. Wolf also teaches

that, even though the oxide material is etched selectively to polysilicon material, some tolerable amount of polysilicon material is etched as well {pages 547-54}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the opening in the oxide layer of Matsuo using an oxide etching treatment as in Wolf since the oxide etching treatment of Wolf would have enabled practitioners of Matsuo to form the openings in the oxide layer, thereby enabling the function of the device to be realized. It also would have been obvious, given the teaching of Wolf, that the layer of conductive material of Matsuo would have been etched to some degree since, even though oxide material may be etched selectively to polysilicon, polysilicon material will still be etched by some tolerable amount. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the contact formed physically in contact with the thick region of Matsuo would have contacted the thick region at a depth deeper than an upper surface of the thick region.

8. Claims 29 and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bergemont, as applied to claims 26, 35, and 36, in view of Chiang et al..

In re claims 29 and 37, Bergemont shows where the first conductive material includes TiN that serves as an interconnect structure and the second conductive material includes a metal that is not TiN {column 8, line 56 – column 10, line 9}.

Bergemont does not show wherein the first conductive material includes polysilicon.

Chiang et al. (herein referred to as Chiang) teaches, in an analogous art related to the field of semiconductor devices, that polysilicon and TiN materials may be used as equivalent materials in formation of interconnect structures {column 6, lines 48-60}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first conductive material of Bergemont using polysilicon instead of TiN since, as

evidenced by Chiang, polysilicon and TiN are well known materials that may be used to form interconnect structures and the selection of a known material on the basis of its suitability for its intended use involves only routine skill in the art.

In re claim 38, Bergemont shows where the first layer includes silicon dioxide and the overlayer includes BPSG {column 8, line 56 – column 10, line 9}.

In re claim 39, Bergemont shows wherein the contact hole is positioned above the opening and the thick region.

Bergemont does not show wherein the contact hole is positioned directly above the opening and the thick region.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the contact hole of Bergemont to have a wider width such that it would enable the contact to be positioned directly above the opening and the thick region since a wider contact hole would allow for better filling and relax lithography tolerances. Additionally, the width of a contact hole is a well known processing variable and the discovery of the optimum or workable dimension of a contact hole involves only routine skill in the art. Furthermore, the specification contains no disclosure of either the critical nature of the claimed contact hole width or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the particular dimensions are critical.

9. Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bergemont, as applied to claim 45 above, in view of Akimoto.

Bergemont further includes forming an overlayer (124) made of an oxide having a thickness over the conductive layer, wherein the conductive layer includes TiN; etching a contact hole through

the overlayer; and forming a contact by filling the contact hole with a conductive material (126) {column 8, line 56 – column 10, line 9}.

Bergemont fails to show wherein an amount of the thick region is etched during the step of etching the contact hole through the overlayer.

Akimoto teaches, in an analogous art related to a method for fabricating a multilayer semiconductor device, that oxide may be etched selectively to TiN material. Akimoto also teaches that, even though the oxide material is etched selectively to TiN material, some tolerable amount of TiN material is etched as well {column 3, lines 1-11}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the opening in the oxide layer of Bergemont using an oxide etching treatment as in Akimoto since the oxide etching treatment of Akimoto would have enabled practitioners of Bergemont to form the openings in the oxide layer, thereby enabling the function of the device to be realized. It also would have been obvious, given the teaching of Akimoto, that the layer of TiN material of Bergemont would have been etched to some degree since, even though oxide material may be etched selectively to TiN, TiN material will still be etched by some tolerable amount.

Response to Arguments

10. Applicant's arguments with respect to claims 21-46 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Paper related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in

Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication of earlier communication from the examiner should be directed to **Kurt Eaton** at **(703) 305-0383** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via kurt.eaton@uspto.gov.

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